UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,527	07/24/2002	Chun-Hsu Lin	8992-US-PA	6640

31561 7590 06/13/2005		EXAMINER
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE		JORGENSEN, LELAND R
7 FLOOR-1, NO. 100		
ROOSEVELT ROAD, SECTION 2	ART UNIT	PAPER NUMBER .
TAIPEI, 100	2675	
TAIWAN		

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AIR MAIL

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/064,527	LIN ET AL.
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 December 2004</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 13* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Objections

1.   In view of applicants amendment filed 8 December 2004, the informality objection to

claims 3, 6, 10, and 13 is withdrawn.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1, 2, 4, 5, 7 – 9, 11, and 12 are rejected under 35 U.S.C. 102(e) as being

anticipated by Shigeta et al, USPN 6,646,625 B1.

Claims 1, 8, and 11

Shigeta teaches a brightness correction apparatus for a plasma display. Shigeta, col. 1,

lines 8 – 10; col. 2, lines 12 – 15. An inverse λ conversion lookup unit [ABL (automatic

brightness control) circuit 31] receives an input signal of a currently displaying pixel [PICEL

DATA D] and converts the input signal into a first gray scale data [brightness-tuning pixel data

D_{BL}] to be output according to an inverse λ conversion rule. Shigeta, col. 9, line 59 – col. 10,

line 34; and figures 6, 7, & 8. An error diffusion unit [error diffusion processing circuit 330 in

multi-level grayscale processing circuit 33], coupled to the inverse λ conversion lookup unit,

receives the first gray scale data, and modifies the first gray scale data into a second gray scale

data recorded as a display brightness error of the currently displaying pixel by considering a

display brightness error of a neighboring pixel of the currently displaying pixel. Shigeta, col. 12,

lines 18 – 26; col. 13, lines 18 – 43; and figures 6, 15, & 16. A gray scale lookup unit [drive

control 2] is coupled to the error diffusion unit to receive an integral portion of the second gray

scale data and to look up a gray scale allocation table [figure 19] to obtain a sustain pulse number

of the currently displaying pixel. Shigeta, col. 3, lines 42 – 46; col. 6, lines 48 – col. 7, line 67;

col. 10, line 45 – 51; and figures 2, 3, & 19.

Claims 2 and 5

Shigeta teaches that the error diffusion unit [multi-level grayscale processing circuit 33]

comprises an adder [332] to receive the first gray scale data to obtain the second gray scale data

by summing the first gray scale data and a weighted display brightness error of the neighboring

pixel. Shigeta, col. 12, line 28 - col. 13, line 14; and figure 15. A brightness error lookup

circuit [data converter circuit 321 and 323] is coupled to the adder to receive the integral portion

of the second gray scale data and to look up a brightness error table [conversion tables in figures

13 and 14] to obtain the brightness error of the currently displaying pixel. Shigeta, col. 11, lines

32 - 36; and figures 10, 13, & 14. A weighted error supply circuit [error diffusion processing

circuit 330] is coupled to the adder and the brightness error lookup circuit to save the brightness

errors of the sequentially displayed currently displaying pixel and the neighboring pixel as the

display brightness errors thereof, and to weight the display brightness error of the neighboring

pixel to obtain the weighted display brightness error required by the adder. Shigeta, col. 13, lines

18 – 43.

Claims 4 and 7

Shigeta teaches that the gray scale allocation includes a lookup table [figure 19] for the

table integral portion of the second gray scale data and the sustain pulse number, and the integral

portion of some different second gray scale data may correspond to the same sustain pulse

number, while the brightness table must be modified to comply with the corresponding

brightness error. Shigeta, col. 3, lines 42 – 46; col. 6, lines 48 – col. 7, line 67; col. 10, line 45

– 51; and figures 2, 3, & 19.

Claim 12

It is inherent that the step of recording the brightness error includes recording a decimal

portion of the second gray scale data.

Claim Rejections - 35 USC § 103

4.   The text of those sections of Title 35, U.S. Code not included in this action can be found

in a prior Office action.

5.   Claims 3, 6, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Shigeta et al., in view of Nagaoka et al. as applied to claims 1, 8, or 11 above, and further in

view of Grossman et al., Advanced Engineering Mathematics (New York: Harper & Row,

1988).

Claims 3, 6, 10, and 13

Shigeta teaches, "Incidentally, in the driving for emitting light, the ratio of the number of

frequencies of light emissions at respective sub-fields SF1 to SF8 is set non-linearly (that is, to

the inverse Gamma ratio, $Y=X^{.2.2}$). This allows the non-linear characteristics (the Gamma

characteristics) of the input pixel data D to be compensated for." Shigeta, col. 11, lines 10 – 15.

Shigeta does not specifically teach that the lookup table for the integral portion of the

second gray scale data G and the brightness error E, and the brightness error table is established

by an actual measured gray scale function of brightness B_0 (G) and an ideal gray scale function

of brightness B(G) as: $E=[(B(G)-B(G_0))/B_0 (G)]*G$.

$[(B(G)-B(G_0))/B_0 (G)]$ is the well known percent error function: the difference between

the actual value and the ideal value divided by the actual value. See e.g. Grossman et al.,

Advanced Engineering Mathematics (New York: Harper & Row, 1988), p. 59.

It would have been obvious to one of ordinary skill in the art at the time of the invention

to combine the percent error function with the brightness correction apparatus of Shigeta to

easily calculate the error.

6.   Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeta in view of

Henlin, USPN 4,708,346.

Claim 9

Shigeta teaches that the error diffusion unit [multi-level grayscale processing circuit 33]

comprises an adder [332] to receive the first gray scale data to obtain the second gray scale data

by summing the first gray scale data and a weighted display brightness error of the neighboring

pixel. Shigeta, col. 12, line 28 - col. 13, line 14; and figure 15. A brightness error lookup

circuit [data converter circuit 321 and 323] is coupled to the adder to receive the integral portion

of the second gray scale data and to look up a brightness error table [conversion tables in figures

13 and 14] to obtain the brightness error of the currently displaying pixel. Shigeta, col. 11, lines

32 - 36; and figures 10, 13, & 14. A weighted error supply circuit [error diffusion processing

circuit 330] is coupled to the adder and the brightness error lookup circuit to save the brightness

errors of the sequentially displayed currently displaying pixel and the neighboring pixel as the

display brightness errors thereof, and to weight the display brightness error of the neighboring

pixel to obtain the weighted display brightness error required by the adder. Shigeta, col. 13, lines

18 – 43.

Shigeta does not specifically teach a subtractor.

Henlin teaches a subtractor. Henlin, col. 1, lines 6 – 45.

It would have been obvious to one of ordinary skill in the art at the time of the invention

to combine the subtractor as taught by Henlin with the brightness correction apparatus as taught

by Shigeta to more quickly add and subtract the neighboring pixel data.

Response to Arguments

7.   Applicant's arguments with respect to claims 1 - 13 have been considered but are moot in

view of the new ground(s) of rejection.

Double Patenting

8.   In view of applicants amendment filed 8 December 2004, the double patenting objection

is withdrawn.

Conclusion

9.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

Hsu et al., USPN 6,774,873 B2, teaches an error diffusion method on a plasma display

panel.

Medina et al., USPN 6,359,389 B1, teaches an gamma function for a flat panel display.

10.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Leland R. Jorgensen whose telephone number is 571-272-7768.

The examiner can normally be reached on Monday through Friday, 10:00 am through 6:00 pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

lrj

DENNIS-DOON CHOW
PRIMARY EXAMINER